REMARKS

In the January 17, 2006 Office Action, the Examiner objected to the drawings, stating that the drawings included reference characters not included in the description. The Examiner also objected to informalities in the specification, requesting removal of the paragraph number from the Abstract and an updated description for pending applications referenced in the specification. As for the claims, the Examiner rejected claims 2-14 under 35 U.S.C. 112, second paragraph, as being indefinite, and rejected claims 1, 5, 7-11, 13-14, 16-18 and 20 under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2004/0034828 to Hocevar (hereinafter "Hocevar") in view of U.S. Patent No. 6,188,699 to Lang et al. (hereinafter "Lang"). However, the Examiner also indicated that claims 2-4 and 12 would be allowable if rewritten to overcome the 35 U.S.C. 112 rejections, and that claims 6, 15, and 19 would be allowable if rewritten in independent form.

Applicants note with appreciation the indication that originally filed claims 2-4, 6, 12, 15 and 19 contain allowable subject matter that would be allowable if rewritten to include the base claim limitations. Because claim 1 has been amended to include the allowable subject matter limitations of claim 2 and to overcome the indefiniteness rejection, Applicants request that the rejection of claims 1 and 3-8 be withdrawn and that the claims be allowed. With respect to the remaining claims, Applicants reserve the right to amend claims 12, 15 and 19 as suggested by the Examiner, but must now respectfully traverse the rejections of claims 9-20 because, as explained more fully below, the Examiner's own analysis confirms that the prior art fails to disclose the data alignment and merger circuitry as claimed.

A. The Objection to the Drawings Is Overcome with 37 CFR § 1.121(b)

In response to the Examiner's objection to the drawings, Applicants have amended the specification to add reference characters in the description in compliance with 37 CFR § 1.121(b). Applicants submit that the addition of the reference characters to the description is not necessary since persons skilled in the art would readily understand the relationship between the identified reference characters in the Figures and the description. However, in order to expedite prosecution of the application, Applicants have made the changes to the description requested by the Examiner, and therefore request that the Examiner reconsider and remove the objection to the drawings.

B. The Specification Has Been Corrected To Overcome the Objections

In response to the Examiner's objection to the Abstract and disclosure at paragraphs 74 and 85, Applicants have amended the Abstract to remove the paragraph number and have updated the description of the referenced patent applications. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the objections to specification.

C. Claims 1, 5, 7-11, 13-14, 16-18 and 20 Are Not Obvious Over Hocevar and Lang

In response to the Examiner's rejection of claims 1, 5, 7-11, 13-14, 16-18 and 20 as being obvious over Hocevar in view of Lang, Applicants respectfully request reconsideration and withdrawal of the rejection for the reasons set forth below.

1. Claims 1 and 3-8 Contain Allowable Subject Matter

As a preliminary matter, claim 1 has been amended to include the allowable subject matter limitations of claim 2 relating to a data merge circuit, and as a result, Applicants respectfully submit that claims 1 and 3-8 are allowable as currently amended.

2. Hocevar Is Non-Analogous Art

As for the Hocevar reference, Applicants submit that the Hocevar's Low Density Parity Check decode circuit is non-analogous prior art which is not in the field of Applicant's endeavor nor reasonably pertinent to the particular problem with which the Applicants are concerned (namely, aligning and merging packet data during memory read and write operations). *See*, MPEP § 2141.01(a). For example, Hocevar's LDPC decoder circuitry 38 is "custom circuitry" for performing decoding of ***incoming*** data packets ***received*** from the RF Circuitry 33 to recover an output bitstream which is forwarded over the bus B to the Host System 30. Hocevar, ¶¶ 49, 52. This seems to be the reverse of Applicants' invention, at least as applied in the Office Action. For example, claim 1 recites a "first interface circuit" for transferring packet data to a "first bus," and also recites a "packet manager circuit" coupled between the first bus and a memory bus for transferring data to the memory bus. According to the Examiner's application of the claim requirements, data is transferred *from* the first bus "B" *to* the memory blocks 252 in the LDPC Decoder Circuitry 38, which is the reverse of the receive decode operations described in Hocevar and depicted in Hocevar Figure 2. Indeed, it does not appear in Hocevar that "packet data" is present at the first bus "B." Nor is it clear if "packet data" is aligned and merged in

Hocevar's LDPC Decoder Circuitry (which the Examiner has identified as containing the claimed alignment circuit).

3. Numerous Requirements of Claims 9-20 Are Not Disclosed In the Art, Including the Differing Data Width Requirements, the Packet Data Coupling Requirements, the Descriptor Offset Requirements, and the Packet Data Fragment Alignment and Merger Requirements

To the extent the Examiner's rejection of claims 9-20 relies on the reasoning behind the rejection of claim 1, Applicants respectfully traverse the Examiner's comparison of the Hocevar reference the claim 1, which recites a packet manager circuit coupled between a first bus (having a first data width) and a memory bus (having a second larger data width). The Examiner has identified a first bus in Hocevar (Figure 2, "B"), but Applicant is not able to ascertain from the Examiner's analysis where Hocevar discloses a "memory bus," much less a memory bus having a larger data width than the first bus ("B"). For example, the Examiner states that a memory bus is disclosed in Hocevar at paragraphs 178 and 181, but the comment in Hocevar that "the circuitry is capable of handling a wide range of code widths" refers to Hocevar's pair parity check update circuits (56a and 56b) in Figure 13. The parity check update circuits have nothing to do with the memory bus. While these passages refer to the different code widths that can be handled by the parity check value estimate memory 52 in the Low Density Parity Check decoding circuitry 38 depicted in Hocevar Figures 1 and 5, there is no disclosure in Hocevar of the relative widths of the first bus and any memory bus.

The packet manager circuit requirements of the present invention are also not disclosed by Hocevar. In particular, the packet manager circuit identified by the Examiner (Hocevar, Figure 2, spread spectrum processor "31") is not coupled between the first bus ("B") and any memory bus in the LDPC decoder circuitry 38, since the "spread spectrum processor 31" in Hocevar includes the LDPC decoder circuitry 38, and is therefore not coupled between the first bus "B" and the LDPC decoder circuitry 38. If anything, the Examiner's analysis of Hocevar is backwards, since Hocevar's transceiver circuit 20 performs LDPC decoding on the received channel input data (provided by the RF Circuitry 33 shown in Figure 2) before transferring the decoded bit stream over the first bus "B" to the host system 30. This is illustrated in attached Exhibit A, which depicts the relationship of the Hocevar alignment circuit (shown in Figure 8) within the LDPC Decoder Circuit 38 (shown in Figure 5) that is contained within the spread-spectrum processor 31 (shown in Figure 2).

There are other deficiencies with the Examiner's proposed analysis of the Hocevar reference. For example, Hocevar does not disclose a "multiprocessor" switching device as recited in claim 1, nor does the Examiner assert as much. Also, the "input buffer" identified by the Examiner (Hocevar, Figure 8, "66A" and "66B) is not coupled to the first bus identified by the Examiner (Hocevar, Figure 2, "B"). In addition, neither Hocevar nor Lang disclose controlling data shifting "in response to an offset" contained in a descriptor, and the Examiner's analysis of Hocevar and Lang is entirely silent on this point.

As for the rejection of claims 9-20, the Examiner summarily invokes the rejection of claim 1. *See*, Office Action, p. 7 (with reference to claims 9 and 16, the Examiner states "see rejection of claim 1"). To the extent the error of this analysis has been set forth above, Applicants traverse the rejection of claims 9-20 for the reasons set forth above. In addition, Applicants respectfully submit that the rejection of claims 9-20 fails to address the distinct claim requirements of these claims. For example, claim 9 recites that the packet manager circuit includes circuitry "*for aligning and merging packet fragments*" which includes a data alignment circuit for "*combining said aligned packet fragments for storage in said output buffer by storing a data fragment from said combined aligned packet fragments in a fragment storage buffer.*" *See*, claim 9 (emphasis added). In view of the Examiner's admission that the prior art do not disclose or make obvious claim 2's recitation of a "data merge circuit" that "combines data stored in the fragment storage register with data stored in the input buffer" (Office Action, p. 8 (emphasis in original)), Applicants respectfully submit that at least the claim 9 requirements (quoted above in italics) are likewise not taught or suggested or made obvious by the prior art. Likewise, the Examiner's admission establishes that the prior art does not disclose or make obvious claim 16's recitation of "aligning and merging packet data" by, *inter alia*, "merging the first shifted data, first fragment data and second shifted data into an output data for transmission to the second bus."

In sum, there is no teaching or suggestion in either Hocevar or Lang to align and merge data using a fragment storage buffer to store an aligned or shifted packet fragment for subsequent combination or merger with another packet fragment. The Examiner appears to have conceded as much with the description of allowable subject matter in claims 2-4, 6, 12, 15 and 19. Accordingly and for at least these reasons, Applicants respectfully request that the rejections of claims 1 and 3-20 be withdrawn and that the claims be allowed.

CONCLUSION

In view of the amendments and remarks set forth herein, Applicants respectfully submits that all pending claims are in condition for allowance. Accordingly, Applicants request that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on April 5, 2006.

Attorney for Applicants

Respectfully submitted,

Michael Rocco Cannatti
Attorney for Applicants
Reg. No. 34,791